

## EDK Abbreviations and Glossary

Abbreviation	Meaning	Description	Where Used/Introduced	Additional Notes:
APU	Auxiliary Processing Unit	Hardware to offload certain functions from the uP used to provide processing acceleration.	Adv – Performance tuning – Section 9.33	
BBD	Black Box Definition	Manages file locations of optimized hardware net lists Used when peripheral is in net list format.		
BFC	Bus Functional Compiler	Translates a BFL file into command that program the selected BFM	Adv – BFM Simulation – Section 12.14	
BFL	Bus Functional Language	Used to describe the behavior of BFM components. Used in simulation	Adv – BFM Simulation – Section 12.14	
BFM	Bus Functional Model	Simplifies and accelerates verification without having to create an exhaustive test bench or full system simulation.	Adv – BFM Simulation – Section 12.7	
BSB	Base System Builder	Wizard that uses an existing BSP to rapidly prototype a project.	Basic – EDK Overview – Section 2	
BMM	Block Memory Map	Contains a syntactic description of how individual block RAMs are used to form a contiguous logical data space.		
BSP	Board Support Package	Contains libraries and available peripherals for a given board.	Adv – Board Support Packages – Section 11	
CacheLink	CacheLink	2 dedicated FSL channels for the uB that connect to the cache controller	Adv – Performance tuning – Section 9.29	
CR	Condition Register	A register internal to the processor that contains the condition results of the last operation executed.	Adv – Performance tuning – Section 9.41	
DCR	Data Control Register	Slow, address limited bus used for configuring peripherals. Occasionally used for data exchange.		
ELF	Executable and Linkable Format	Final stage of the software process. Next step it to merge into BRAM.		
DUT	Device Under Test	The device begin tested or simulated	Adv – BFM Simulation – Section 12.7	See also UUT
FCB	Fabric Co-processor Bus	Dedicated bus that provides a standard interface between the APU and FCM (optional)	Adv – Performance tuning – Section 9.37	
FCM	Fabric Co-processor Module	Specialized hardware in FPGA fabric that is coupled to the APU in the PPC.	Adv – Performance tuning – Section 9.36	
FSL	Fast Simplex Link	FIFOs that directly connect the processor to the FPGA fabric. The uB supports 8 FSLs (32 bits wide). The PPC supports 32 FSL via the APU.	Adv – Performance tuning – Section 9.21	FSL Bus Data Sheet DS449
GDB	GNU Debugger	Basic monitor program to observe program execution and effect	Basic – section 12	
GPR	General Purpose Register	A register internal to the processor used for storing temporary data.	Adv – Performance tuning – Section 9.41	
LibGen	Library Generator	SW tool that generates libraries and drivers for embedded processors.		
MDD	Microprocessor Driver Definition	Contains directives for customizing software drivers.		
MHS	Microprocessor Hardware Specification	Describes all the devices to be instantiated and their new values, address space, connections, etc. from a hardware perspective. Over-rides the .MPD file.		
MLD	Microprocessor Library Definition	SW that customizes a BSP to specific OS requirements. Comprised of a data definition file and data generation file.	Adv – Board Support Packages – Section 11.34	
MPD	Microprocessor Peripheral Description	Contains the default values for all aspects of a peripheral – ports, parameters, and buses		
MSS	Microprocessor Software Specification	Describes the software environment including operating system, clock speed, etc.		
OPB	On-chip Peripheral Bus			Both PPC and uB
PAO	Peripheral Analyze Order	Contains a list of HDL files that are needed for synthesis and defines the analysis order for compilation. Used when peripheral is in HDL format.		
PlatGen	Platform Generator	SW tool that creates an implementation net list of a bus-based subsystem.		
PLB	Processor Local Bus			PPC Only
SVF	Serial Vector File	Specific format used for programming SystemAce	Adv – Bootloader – Section 14-11	
SimGen	Simulation Generator	SW tool that creates a simulation environment.		
UCF	User Constraint File	Describes pin connections and timing constraints.		
UDI	User Defined Instruction	Special instruction in the PPC that defers interpretation to the Co-Processor.	Adv – Performance tuning – Section 9.41	
UUT	Unit Under Test	The device begin tested or simulated	Adv – BFM Simulation – Section 12.7	See also DUT
XBD	Xilinx Board Definition			
XMD	Xilinx Microprocessor Debugger	Forms connection between the cable and the GDB	Basic – section 12	
XMD Stub	Xilinx Microprocessor Debugger Stub	Software that resides in the Microprocessor's program space that enables connection to the XMD running on the development platform.	Basic – section 12	
XMK	Xilinx Micro-Kernel	Xilinx's own small RTOS kernel	Adv – Board Support Packages – Section 11.27	
XMP	Xilinx Microprocessor Project	Defines information critical to a given project.		
XPS	Xilinx Platform Studio	Development Environment for specifying hardware and software for a given embedded project.		