

Course Description

The course provides a thorough introduction to the Vivado® High-Level Synthesis (HLS) tool. This course covers synthesis strategies, features, improving throughput, area, interface creation, latency, testbench coding, and coding tips. Utilize the Vivado HLS tool to optimize code for high-speed performance in an embedded environment and download for in-circuit validation.

Level – DSP 3

Course Duration – 2 days

Price –

Course Part Number – DSP-HLS-ILT

Who Should Attend? – Software and hardware engineers looking to utilize high-level synthesis

Prerequisites

- C, C++, or System C knowledge
- High-level synthesis for software engineers OR high-level synthesis for hardware engineers

Software Tools

- Vivado System Edition 2015.3

Hardware

- Architecture: Zynq®-7000 All Programmable SoC and 7 series FPGAs*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 All Programmable SoC and 7 series FPGA architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Enhance productivity using the Vivado HLS tool
- Describe the high-level synthesis flow
- Use the Vivado HLS tool for a first project
- Identify the importance of the testbench
- Use directives to improve performance and area and select RTL interfaces
- Identify common coding pitfalls as well as methods for improving code for RTL/hardware
- Perform system-level integration of IP generated by the Vivado HLS tool
- Describe how to use OpenCV functions in the Vivado HLS tool

Course Outline

Day 1

- Introduction to High-Level Synthesis and the Vivado HLS Tool
- Using the Vivado HLS Tool: GUI Flow
- Demo: Vivado HLS Tool Overview
- **Lab 1:** Introduction to the Vivado HLS Tool Flow
- Vivado HLS Tool Command Line Interface
- **Lab 2:** Introduction to the Vivado Tool HLS CLI Flow
- Optimizing for Latency
- **Lab 3:** The Impact of Unrolling Loops
- Optimizing for Throughput
- **Lab 4:** Optimizing for Throughput

Day 2

- Optimizing Arrays
- **Lab 5:** Handling Memories
- Optimizing for Area
- I/O Interfaces
- Demo: AXI4-Streaming Interfaces
- **Lab 6:** System Integration
- HLS UltraFast Design Methodology
- Vivado HLS Tool: C Code
- **Lab 7:** Matrix Multiplication

Lab Descriptions

- **Lab 1:** Introduction to the Vivado HLS Tool Flow – Utilize the GUI to simulate and create a project. Perform RTL synthesis, verification, and exporting the C design as an IP.
- **Lab 2:** Introduction to the Vivado HLS Tool CLI Flow – Utilize a make file to perform C simulation. Create a project and perform C synthesis, RTL verification, and RTL packaging.
- **Lab 3:** The Impact of Unrolling Loops – Analyze multiple results of the design and apply directives to optimize loop latency.
- **Lab 4:** Optimizing for Throughput – Optimize loop performance and modify pipelining and its effect on performance.
- **Lab 5:** Handling Memories – Analyze the impact of manipulating arrays. Utilize directives to optimize the design for area.
- **Lab 6:** System Integration – Set up an embedded design, create an HLS IP with the AXI Lite interface, import the IP into the embedded design, and validate the system on the demo board.
- **Lab 7:** Matrix Multiplication – Write a C-code 3x3 matrix multiplier, verify the design, and apply directives to improve performance.

Register Today

Xilinx's network of Authorized Training Providers (ATP) delivers public and private courses in locations throughout the world. Please contact your closest ATP for more information, to view schedules, or to register online.

Visit www.xilinx.com/training and click on the region where you want to attend a course.

Americas, contact your training provider at www.xilinx.com/training/atp.htm#NA or send your inquiries to registrar@xilinx.com.

Europe, contact your training provider at www.xilinx.com/training/atp.htm#EU or send your inquiries to eurotraining@xilinx.com.

Asia Pacific, contact your training provider at www.xilinx.com/training/atp.htm#AP, or send your inquiries to education_ap@xilinx.com, or call +852-2424-5200.

Japan, contact your training provider at www.xilinx.com/training/atp.htm#JP, or send your inquiries to education_kk@xilinx.com, or call +81-3-6744-7970.